



PJSMDA05 SERIES

QUAD TVS/ZENER ARRAY FOR ESD AND LATCH-UP PROTECTION

This Quad TVS/Zener Array family have been designed to Protect Sensitive Equipment against ESD and to prevent Latch-Up events in CMOS circuitry operating at 5V,12V,15V and 24V.

This TVS array offers an integrated solution to protect up to 4 data lines where the board space is a premium.

FEATURES

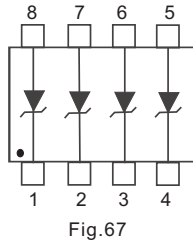
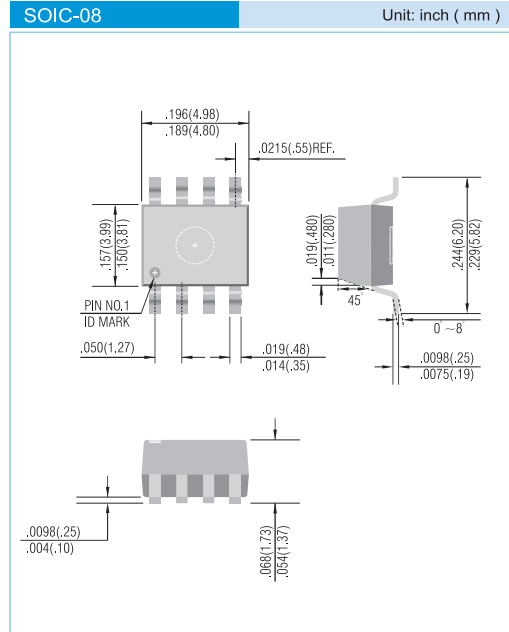
- 350W Power Dissipation (8/20 μ s Waveform)
- Low Leakage Current, Maximum of 5 μ A at rated voltage
- Very Low Clamping Voltage
- IEC61000-4-2 ESD 20kV air,15kV Contact Compliance
- In compliance with EU RoHS 2002/95/EC directives

MECHANICAL DATA

- Case: SOIC-08, Molded plastic over passivated junction
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.079 grams
- Mounting Position : Any

APPLICATIONS

- RS-232C or RS-422 Communication ports
- GPIB/IEEE 485 Ports
- Portable Instrumentation



MAXIMUM RATINGS (Per Device)

Rating	Symbol	Value	Units
Peak Pulse Power (8/20 μ s Waveform)	P _{PP}	350	W
ESD Voltage (HBM) Per MIL-STD-883C	V _{ESD}	>25	kV
Operating Temperature Range	T _J	-50 to +150	°C
Storage Temperature Range	T _{STG}	-50 to +150	°C



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ELECTRICAL CHARACTERISTICS (PER DEVICE) T_J = 25°C

PJSMDA05 Marking DA5						
Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V _{RWM}		-	-	5	V
Reverse Breakdown Voltage	V _{BR}	I _{BR} =1mA	6	-	-	V
Reverse Leakage Current	I _R	V _R =5V	-	-	5	μA
Clamping Voltage (8/20μs)	V _C	I _{PP} =5A	-	-	9.8	V
Clamping Voltage (8/20μs)	V _C	I _{PP} =24A	-	-	13	V
Off State Junction Capacitance	C _J	0 Vdc Bias f=1MHz	-	400	500	pF
Off State Junction Capacitance	C _J	5 Vdc Bias f=1MHz	-	200	250	pF
PJSMDA12 Marking DA2						
Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V _{RWM}		-	-	12	V
Reverse Breakdown Voltage	V _{BR}	I _{BR} =1mA	13.3	-	-	V
Reverse Leakage Current	I _R	V _R =5V	-	-	5	μA
Clamping Voltage (8/20μs)	V _C	I _{PP} =5A	-	-	20	V
Clamping Voltage (8/20μs)	V _C	I _{PP} =15A	-	-	25	V
Off State Junction Capacitance	C _J	0 Vdc Bias f=1MHz	-	-	300	pF
PJSMDA15 Marking DAA						
Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V _{RWM}		-	-	15	V
Reverse Breakdown Voltage	V _{BR}	I _{BR} =1mA	16.7	-	-	V
Reverse Leakage Current	I _R	V _R =5V	-	-	5	μA
Clamping Voltage (8/20μs)	V _C	I _{PP} =5A	-	-	24	V
Clamping Voltage (8/20μs)	V _C	I _{PP} =12A	-	-	29	V
Off State Junction Capacitance	C _J	0 Vdc Bias f=1MHz	-	-	200	pF
PJSMDA24 Marking DA4						
Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V _{RWM}		-	-	24	V
Reverse Breakdown Voltage	V _{BR}	I _{BR} =1mA	26.7	-	-	V
Reverse Leakage Current	I _R	V _R =5V	-	-	5	μA
Clamping Voltage (8/20μs)	V _C	I _{PP} =5A	-	-	40	V
Clamping Voltage (8/20μs)	V _C	I _{PP} =8A	-	-	44	V
Off State Junction Capacitance	C _J	0 Vdc Bias f=1MHz	-	-	120	pF

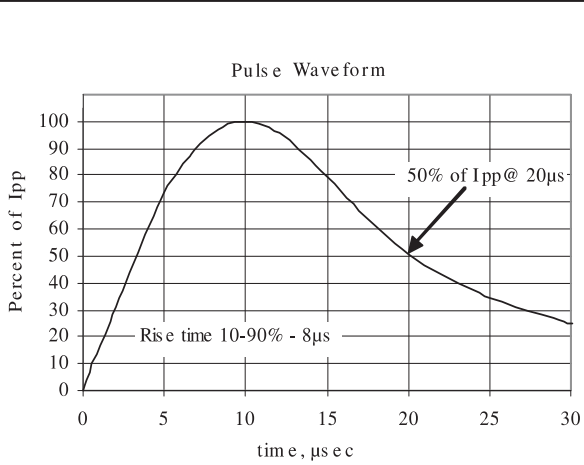
PRELIMINARY



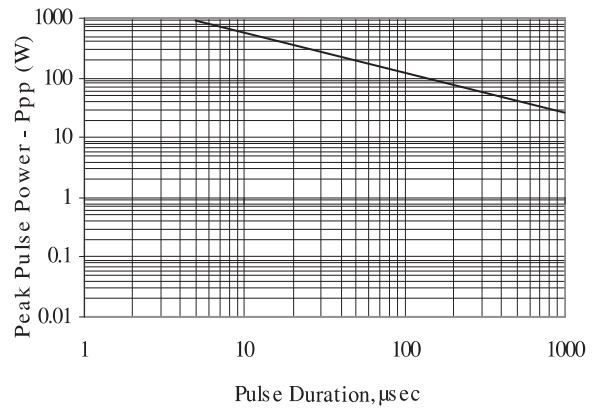
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TYPICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$ unless otherwise noted

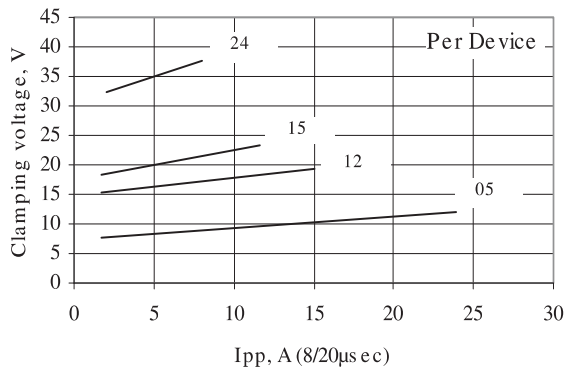
Surge Pulse Waveform Definition



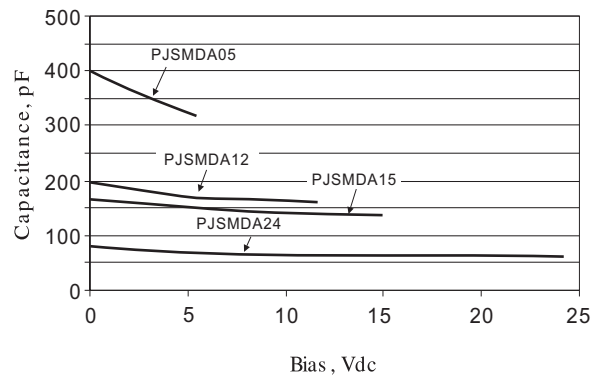
Non-Repetitive Peak Pulse Power vs Pulse Time



Clamping Voltage vs. Peak current



Off-State Capacitance per Device - 1MHz

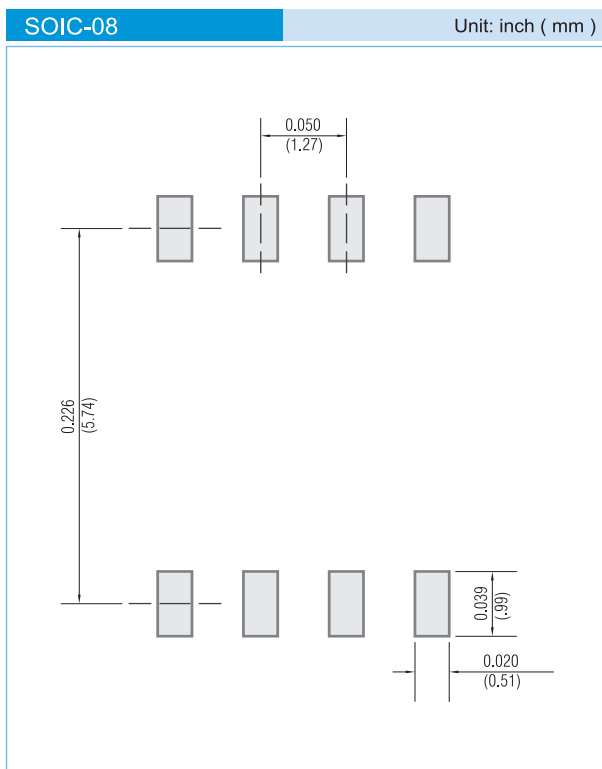


PRELIMINARY



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MOUNTING PAD LAYOUT



ORDER INFORMATION

- Packing information
T/R - 3K per 13" plastic Reel

LEGAL STATEMENT

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