



# PJA3415AE

## 20V P-Channel Enhancement Mode MOSFET – ESD Protected

**Voltage**

**-20 V**

**Current**

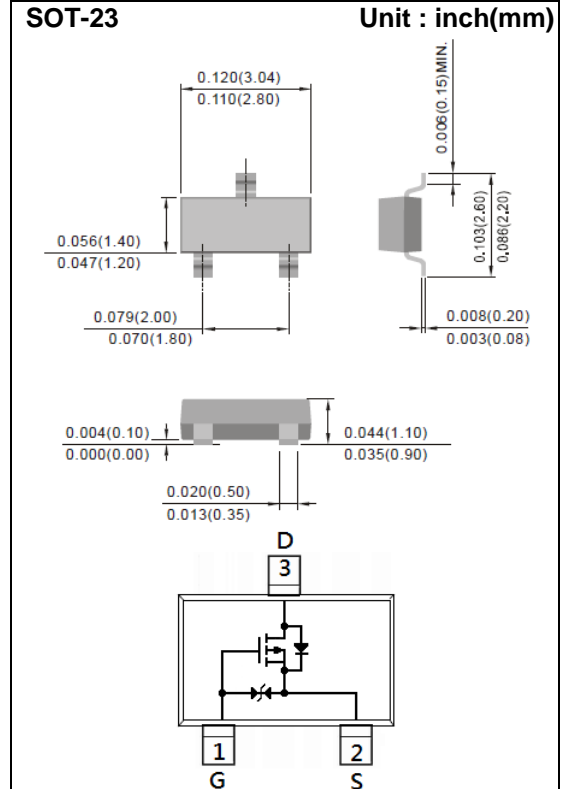
**-4.3A**

### Features

- $R_{DS(ON)}$ ,  $V_{GS}@-4.5V$ ,  $I_D@-4.3A < 50m\Omega$
- $R_{DS(ON)}$ ,  $V_{GS}@-2.5V$ ,  $I_D@-4.0A < 58m\Omega$
- $R_{DS(ON)}$ ,  $V_{GS}@-1.8V$ ,  $I_D@-2.4A < 73m\Omega$
- Advanced Trench Process Technology
- Specially Designed for Switch Load, PWM Application, etc
- ESD Protected 2KV HBM
- Lead free in compliance with EU RoHS 2011/65/EU directive
- Green molding compound as per IEC61249 Std.

### Mechanical Data

- Case: SOT-23 Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0003 ounces, 0.0084 grams
- Marking: A5AE



### Maximum Ratings and Thermal Characteristics ( $T_A=25^\circ C$ unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNITS
Drain-Source Voltage	$V_{DS}$	-20	V
Gate-Source Voltage	$V_{GS}$	$\pm 8$	V
Continuous Drain Current	$I_D$	-4.3	A
Pulsed Drain Current	$I_{DM}$	-17.2	A
Power Dissipation	$P_D$	$T_a=25^\circ C$	1.25
		Derate above $25^\circ C$	10
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55~150	$^\circ C$
Typical Thermal resistance	$R_{\theta JA}$	100	$^\circ C/W$
- Junction to Ambient (Note 3)			



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## Electrical Characteristics ( $T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
<b>Static</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-20	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.4	-0.55	-1.0	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-4.3A$	-	42	50	mΩ
		$V_{GS}=-2.5V, I_D=-4.0A$	-	49	58	
		$V_{GS}=-1.8V, I_D=-2.4A$	-	59	73	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-20V, V_{GS}=0V$	-	-0.01	-1	μA
Gate-Source Leakage Current	$I_{GSS}$	$V_{GS}=\pm 8V, V_{DS}=0V$	-	$\pm 6$	$\pm 10$	μA
<b>Dynamic</b> (Note 5)						
Total Gate Charge	$Q_g$	$V_{DS}=-10V, I_D=-4.3A,$ $V_{GS}=-4.5V$ (Note 1,2)	-	24	-	nC
Gate-Source Charge	$Q_{gs}$		-	1.5	-	
Gate-Drain Charge	$Q_{gd}$		-	2.5	-	
Input Capacitance	$C_{iss}$	$V_{DS}=-10V, V_{GS}=0V,$ $f=1.0\text{MHz}$	-	907	-	pF
Output Capacitance	$C_{oss}$		-	90	-	
Reverse Transfer Capacitance	$C_{rss}$		-	70	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=-10V, I_D=-4.3A,$ $V_{GS}=-4.5V,$ $R_G=6\Omega$ (Note 1,2)	-	45	-	ns
Turn-On Rise Time	$t_r$		-	79	-	
Turn-Off Delay Time	$t_{d(off)}$		-	193	-	
Turn-Off Fall Time	$t_f$		-	826	-	
<b>Drain-Source Diode</b>						
Maximum Continuous Drain-Source Diode Forward Current	$I_S$	---	-	-	-1.5	A
Diode Forward Voltage	$V_{SD}$	$I_S=-1.0A, V_{GS}=0V$	-	0.76	-1.2	V

NOTES :

1. Pulse width  $\leq 300\mu s$ , Duty cycle  $\leq 2\%$
2. Essentially independent of operating temperature typical characteristics.
3.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins mounted on a 1 inch FR-4 with 2oz. square pad of copper
4. The maximum current rating is package limited
5. Guaranteed by design, not subject to production testing.



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## TYPICAL CHARACTERISTIC CURVES

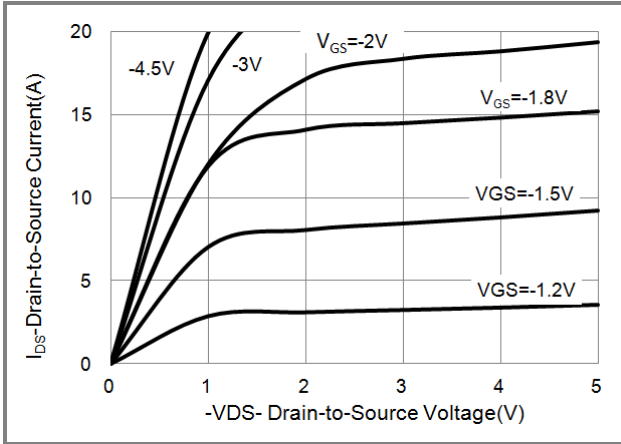


Fig.1 On-Region Characteristics

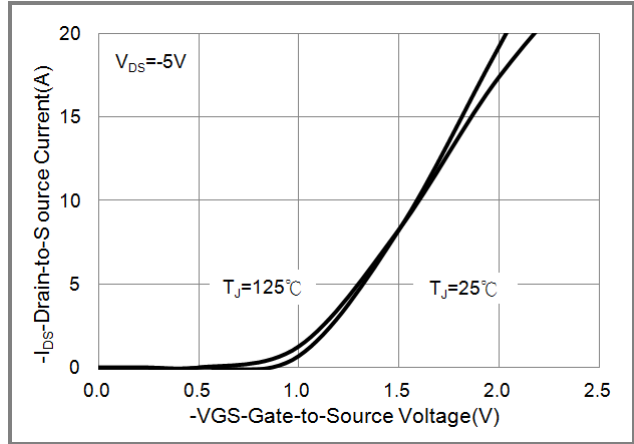


Fig.2 Transfer Characteristics

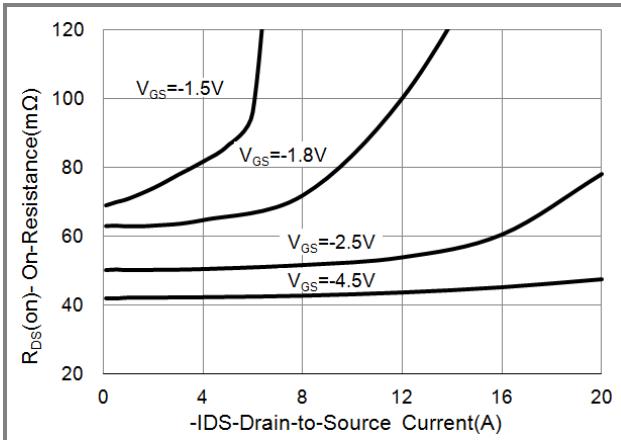


Fig.3 On-Resistance vs. Drain Current

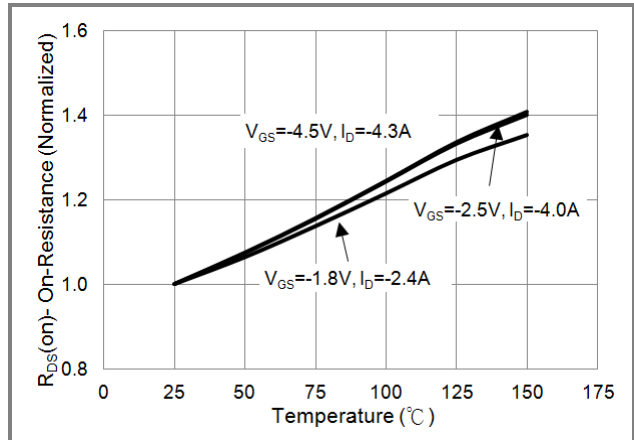


Fig.4 On-Resistance vs. Junction temperature

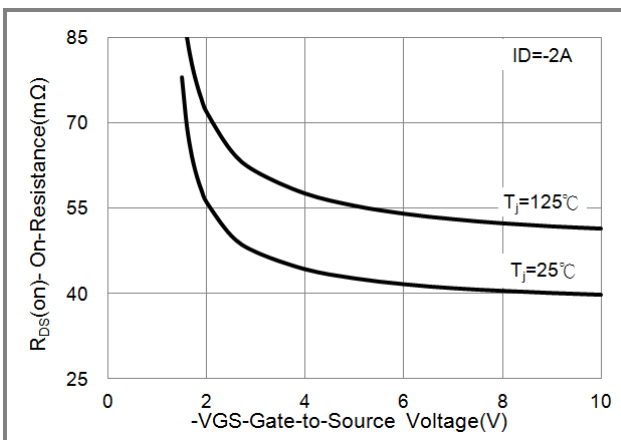


Fig.5 On-Resistance Variation with VGS.

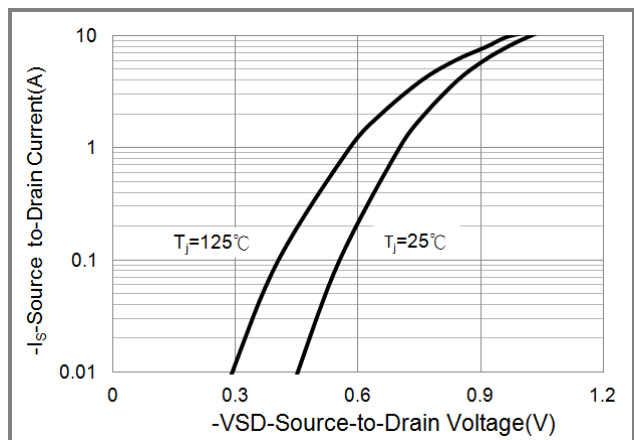


Fig.6 Body Diode Characteristics



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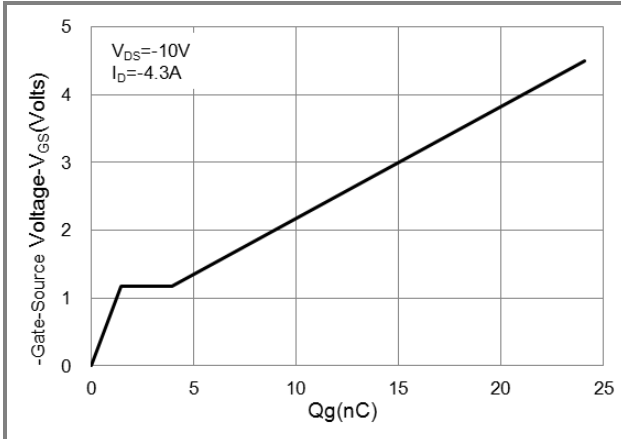


Fig.7 Gate-Charge Characteristics

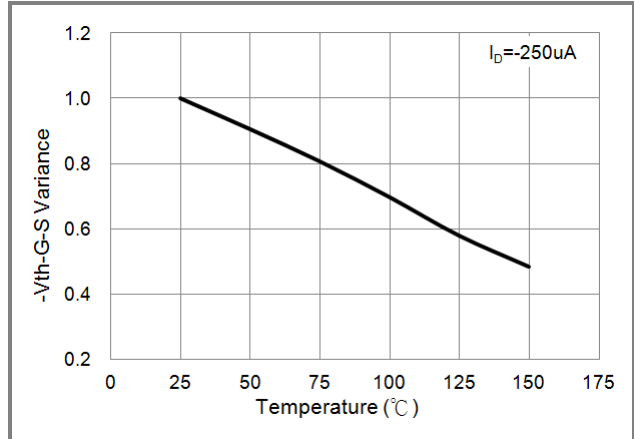


Fig.8 Threshold Voltage Variation with Temperature.

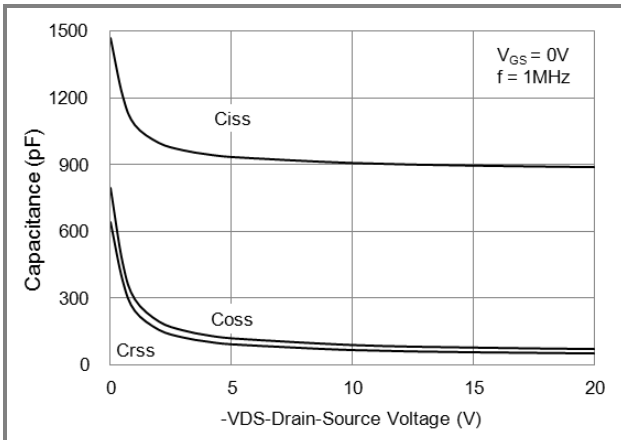


Fig.9 Capacitance vs. Drain-Source Voltage.